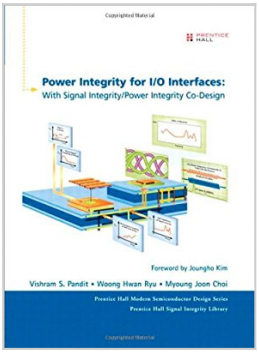

Power Integrity for I/O Interfaces: With Signal Integrity/ Power Integrity Co-Design (Prentice Hall Modern Semiconductor Design)

By Vishram S. Pandit, Woong Hwan Ryu, Myoung Joon Choi

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Foreword by Joungho Kim

The Hands-On Guide to Power Integrity in Advanced Applications, from Three Industry Experts

In this book, three industry experts introduce state-of-the-art power integrity design techniques for today's most advanced digital systems, with real-life, system-level examples. They introduce a powerful approach to unifying power and signal integrity design that can identify signal impediments earlier, reducing cost and improving reliability.

After introducing high-speed, single-ended and differential I/O interfaces, the authors describe on-chip, package, and PCB power distribution networks (PDNs) and signal networks, carefully reviewing their interactions. Next, they walk through end-to-end PDN and signal network design in frequency domain, addressing crucial parameters such as self and transfer impedance. They thoroughly address modeling and characterization of on-chip components of PDNs and signal networks, evaluation of power-to-signal coupling coefficients, analysis of Simultaneous Switching Output (SSO) noise, and many other topics.

Coverage includes
• The exponentially growing challenge of I/O power integrity in high-speed digital systems
• PDN noise analysis and its timing impact for single-ended and differential interfaces
• Concurrent design and co-simulation techniques for evaluating all power integrity effects on signal integrity
• Time domain gauges for designing and optimizing components and systems
• Power/signal integrity interaction mechanisms, including power noise coupling onto signal trace and noise amplification through signal resonance

• Performance impact due to Inter Symbol Interference (ISI), crosstalk, and SSO noise, as well as their interactions
• Validation techniques, including low impedance VNA measurements, power noise measurements, and characterization of power-to-signal coupling effects

Power Integrity for I/O Interfaces will be an indispensable resource for everyone concerned with power integrity in cutting-edge digital designs, including system design and hardware engineers, signal and power integrity engineers, graduate students, and researchers.

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PREFACE

Power Integrity is becoming increasingly important in today's high-speed digital I/O systems. The cover of this book gives a high-level summary of its system impact. It shows an electronic system with a Printed Circut Board (PCB), a daughter card, and their layer stackup. A driver chip is mounted on the PCB and a receiver chip is mounted on the daughter card. The expanded view of the power grid of the driver chip is also shown. The receiver jitter impact is due to Power Delivery (PD) to signal coupling, and there are different coupling mechanisms. Self impedance response of the PDN at the driver chip shows a resonance in the mid-frequency range. The PD to signal coupling response at the driver chip follows the PDN self impedance response. The jitter at the receiver follows a similar signature at those frequencies when the transmission line effect is negligible. The PD to signal coupling at the package to PCB interface increases as the frequency goes higher. The channel response shows resonances at high frequencies, due to impedance discontinuities. The power to signal coupling noise can get amplified due to the channel effects and resonances. This, in turn, gets translated into jitter at the receiver at high frequencies. Referencing scheme, such as dual referencing, also causes the PD to signal coupling.

Intended audience for this book is Signal Integrity (SI) and Power Integrity (PI) Engineers (On-chip, package, and PCB designers). It can also be used by graduate students who want to pursue careers in these fields. Overall discussion level is beginner to intermediate; however, some advanced topics are also discussed. There may be different designers working on specific components, such as on-chip or package or PCB. However, this book presents power integrity design techniques along with power-to-signal coupling mechanisms at various stages in the system, such as chip level coupling and interconnect level coupling. This will give the component SI or PI engineers a perspective of system level impact of power integrity, and enable them to proactively design the system to avoid possible problem areas and also to identify the root-cause, in case of any system problems.

Chapter 1, "Introduction," describes digital electronic systems and gives a high-level overview of the PDN and signal network. It describes signal and power integrity effects on system performance and highlights power noise to signal coupling mechanisms. Finally, it addresses the need for concurrent SI/PI design methodology.

Chapter 2, "I/O Interfaces," describes basic Input Output interfaces. The currents in power node generate noise that is basis of power integrity effects for I/O interfaces. This chapter addresses details of single-ended and differential drivers and receivers. Single-ended and differential interfaces produce different current profiles in the PDN, and their dependency on the bit pattern is also different. The PDN current flows are demonstrated with corresponding noise.

Chapter 3, "Electromagnetic Effects," discusses the electromagnetic (EM) theory and how it is important in signal integrity, power integrity and ElectroMagnetic Interference (EMI) analysis. It begins with basic Maxwell's equations, and addresses transmission line theory and interconnect network parameters (Z, Y, S). It also describes Linear Time Invariant (LTI) systems and their properties.

Chapter 4, "System Interconnects," addresses the entire path for power and signal propagation, including the chip, package, and PCB. It gives an overview of the PCB technology and different package types. In the PDN section it describes PCB PDN components (DC/DC converter, PCB capacitors, PCB planes, vias, and so forth), package PDN, and on-chip PDN components (intentional/unintentional capacitors, and power-grid). In the signal network section, it describes PCB signal propagation with microstrip, stripline, and coupled line. It also addresses the package and on-chip signal networks. Then, it states the coupling mechanism from the PDN to signal network. Finally, it addresses modeling tools for the PDN and signal

networks.

Chapter 5, “Frequency Domain Analysis,” begins with Fourier transform and its properties. It lists the key frequency domain design parameters for signal integrity and power integrity applications. It then addresses frequency domain PDN design with Z_{11} impedance target. It utilizes chip, package, and PCB co-design approach for the PDN design. Some important frequency domain concepts in the PDN design, such as voltage transfer function, SSO in frequency domain, and power to signal coupling, are illustrated. The next section describes the frequency domain signal network analysis and its correlation. A case study for “crosstalk amplification by resonance” is discussed in detail. The signal network analysis is performed with the PDN and on-chip parameters (on-die termination, pad capacitor, and so on) taken into account. Differential signaling parameters in frequency domain are also presented.

Chapter 6, “Time Domain Analysis,” begins with describing the necessary components for the time domain simulations. It addresses various kinds of buffer models used in signal integrity and power integrity analysis. Next, it describes the time domain PDN specifications, and simulation flow to achieve the specifications. Different examples of single ended drivers and differential drivers are presented for AC noise analysis. Next, the concept of chip level driver noise coupling on the signal is discussed. It shows examples of the jitter analysis due to the PDN noise, for single ended and differential interfaces.

Chapter 7, “Signal/Power Integrity Interactions,” is devoted to unintended interactions between power/ground and signals, which has become an important consideration for optimizing high-bandwidth I/O signaling scheme. Power noise coupling can be amplified through channel resonance. It describes the power noise amplification mechanism that is due to a combination of three factors: SSO generation, power to signal coupling, and signal channel resonance. Then two case studies are demonstrated: DDR2-800 control bus resonance problem and DDR2667 Vref bus noise issue. Next, it describes the referencing/stitching/and decoupling effects for single ended and differential interfaces.

Chapter 8, “Signal/Power Integrity Co-Analysis,” addresses the eye-margin analysis with SI-PI co-simulations. It describes the basic elements for the cosimulations: buffer models, 3D EM models for package and PCB, on-chip PDN models, and so on. The simulation deck is constructed and the worst case pattern is identified. Full-time domain simulations are performed with ISI, crosstalk, and SSO analysis; and response decomposition techniques are illustrated. The linear interaction indicator between power and signal is defined and evaluated for single ended and differential interfaces.

Chapter 9, “Measurement Techniques,” covers the frequency domain and time domain measurement techniques for validating signal/power integrity, in high-speed I/O signaling. The theory and some applications of the enhanced 2-port VNA technique for low impedance power delivery network characterization are discussed in the first part of this chapter. It also describes the on-chip interconnect and pad capacitance characterization techniques. In addition, it presents S-parameter measurement-based extraction methods to obtain the high-frequency SPICE model, with microwave network analysis and parametric optimization. Next, it describes the time domain characterization techniques. It includes Time Domain Reflectometry (TDR) measurement, PDN noise measurement, SSO coupling measurement, and jitter measurement.

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